

Appl. No. 10/710,175
Amdt. dated July 11, 2006
Reply to Office action of April 11, 2006

Amendments to the Specification

Please replace the section entitled "Brief Description of Drawings" with the following amended paragraph:

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Fig.1 shows the block diagram of a typical apparatus for generating a phase delay.

Fig.2 is a functional block diagram of an apparatus for generating a phase delay according to an embodiment of the claimed invention.

Fig.3 is a flowchart of a delaying process employed by the apparatus for generating a phase delay according to an embodiment of the claimed invention.

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Fig.4 is a functional block diagram of an apparatus for adjusting the phase difference between two input signals according to an embodiment of the claimed invention.

15 Please insert a new paragraph [0026.1] between original paragraphs [0026] and [0027]:

[0026.1] As mentioned above, two or more of the circuits shown in Fig.2 can be implemented at the same time. An example is illustrated as below. Please refer to Fig.4. Fig.4 is a functional block diagram of an apparatus 400 for adjusting the phase difference between two input signals according to an embodiment of the claimed invention. The apparatus 400 comprises: a first adjusting circuit 405, comprising a first buffer 410, a first DAC 420, and a first variable capacitor 430; and a second adjusting circuit 445, comprising a second buffer 440, a second DAC 450, and a second variable capacitor 460. In this embodiment, the first adjusting circuit 405 and the second adjusting circuit 445 can respectively adjust the phases of a first input signal and a second input signal in order to adjust the phase difference between the input signals, wherein the first input signal and the second input signal may be a pair of differential signals, or I/Q signals. This embodiment may further be implemented in a receiver, a transmitter, or a transceiver. As

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in the circuit shown in Fig.2, the first variable capacitor and the second variable capacitor can be voltage-controlled capacitors, such as MOS-based voltage-controlled capacitors or P+/N well junction voltage-controlled capacitors. These modifications all fall within the scope of the present invention.

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